WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a bank having a plurality of arrayed memory cells;

a bus line transmitting data read from the bank, and having a line equivalent to one word;

a plurality of sense amplifiers detecting data read from a memory cell of the bank in accordance with a read address;

a plurality of first holding circuits individually holding data output from each of the sense amplifiers;

a plurality of second holding circuits individually holding data output from each of the first holding circuits, and holding data output from the corresponding first holding circuit after being delayed by time that the read address gains with respect to burst address; and

a decoder supplying data held in said plurality of second holding circuits to the corresponding line of the bus line.

2. The device according to claim 1, further comprising:

a delay circuit generating a control signal of the second holding circuit, the delay circuit generating the control signal by delaying the read address by time that the read address gains with respect to the burst address in accordance with a clock signal.

3. The device according to claim 1, wherein the

first holding circuit comprises an asynchronous latch circuit, and the second holding circuit comprises a synchronous latch circuit.

4. A semiconductor memory device comprising:

a first bank having a plurality of arrayed memory cells;

a second bank having a plurality of arrayed memory cells:

first and second output circuits provided correspondingly to the first and second banks, the first and second output circuits outputting data read from the corresponding said plurality of memory cells in accordance with read address, and being activated after being delayed by time that the read address gains with respect to the burst address when select is changed from one of the first and second banks to the other thereof; and

a select circuit selecting the first and second output circuits, the select circuits selecting one of the first and second banks after being delayed by time that the read address gains with respect to the burst address when select is changed from one of the first and second banks to the other thereof.

5. The device according to claim 1, further comprising:

a first bus line transmitting data read from the first bank, and having a bit width equivalent to one

word;

a second bus line transmitting data read from the second bank, and having a bit width equivalent to one word;

a plurality of first sense amplifiers detecting data read from a memory cell of the first bank in accordance with the read address;

a plurality of second sense amplifiers detecting data read from a memory cell of the second bank in accordance with the read address;

a plurality of first holding circuits individually holding data output from the first sense amplifiers;

a plurality of second holding circuits individually holding data output from the second sense amplifiers;

a plurality of third holding circuits individually holding data output from the first holding circuits after being delayed by time that the read address gains with respect to the burst address;

a plurality of fourth holding circuits individually holding data output from the second holding circuits after being delayed by time that the read address gains with respect to the burst address;

a first decoder supplying data held in said plurality of third holding circuits to the corresponding first bus line;

a second decoder supplying data held in said

plurality of fourth holding circuits to the corresponding second bus line; and

a bank select signal generator circuit outputting one bank data of the first and second banks, and thereafter, generating a signal for generating the other bank data after being delayed by time that the read address gains with respect to the burst address.

6. The device according to claim 4, further comprising:

a delay circuit delaying the read address by time that the read address gains with respect to the burst address in accordance with a clock signal, and generating control signals of the third and fourth holding circuits.

7. The device according to claim 4, wherein the bank select signal generator is a delay circuit for delaying a bank select signal by time that the read address gains with respect to the burst address in accordance with a clock signal.

8. The device according to claim 5, wherein the first and second holding circuits comprise an asynchronous latch circuit, and the third and fourth holding circuits comprise a synchronous latch circuit.

9. A semiconductor memory device comprising:

a first bank having a plurality of arrayed memory cells;

a second bank having a plurality of arrayed memory

cells:

a redundancy memory having a plurality of memory cells storing data of defective block of the first and second banks;

an address memory storing an address of the defective block;

a comparator comparing an address for reading one data of the first and second banks with the address of the defective block stored in the address memory, and outputting a coincidence signal if the former address and the later address coincide with each other; and

a selector circuit selecting the redundancy memory after being delayed by time that the read address gains with respect to the burst address when the comparator outputs the coincidence signal.

10. The device according to claim 9, further comprising:

a first bus line transmitting data read from the first bank, and having a bit width equivalent to one word;

a second bus line transmitting data read from the second bank and the redundancy memory, and having a bit width equivalent to one word;

a plurality of first sense amplifiers detecting data read from a memory cell of the first bank in accordance with the read address;

a plurality of second sense amplifiers detecting

data read from one of memory cells of the second bank and the redundancy memory in accordance with the read address;

a plurality of first holding circuits individually holding data output from said plurality of first sense amplifiers;

a plurality of second holding circuits individually holding data output from said plurality of second sense amplifiers;

a plurality of third holding circuits individually holding data output from the first holding circuits after being delayed by time that the read address gains with respect to the burst address;

a plurality of fourth holding circuits individually holding data output from the second holding circuits after being delayed by time that the read address gains with respect to the burst address, and individually holding data output from the second holding circuits after being delayed by time that the read address gains with respect to the burst address when the comparator circuit outputs the coincidence signal;

a first decoder supplying data held in said plurality of third holding circuits to the corresponding first bus line;

a second decoder supplying data held in said plurality of fourth holding circuits to the

corresponding second bus line; and

an output circuit connected to the first and second bus lines, outputting one bank data of the first and second banks when the comparator outputs the coincidence signal, and thereafter, outputting data of the redundancy memory after being delayed by time that the read address gains with respect to the burst address.

11. The device according to claim 10, wherein the first and second holding circuits comprise an asynchronous latch circuit, and the third and fourth holding circuits comprise a synchronous latch circuit.

12. A semiconductor memory device comprising:

a bank having a plurality of arrayed memory cells;

a first bus line transmitting even data read from the bank, and having a bit width equivalent to one word;

a second bus line transmitting odd data read from the bank and the redundancy memory, and having a bit width equivalent to one word;

a plurality of first sense amplifiers detecting even data read from a memory cell of the bank in accordance with read address;

a plurality of second sense amplifiers detecting odd data read from the memory cell of the bank in accordance with read address;

a plurality of first holding circuits individually

holding data output from each of the first sense amplifiers;

a plurality of second holding circuits individually holding data output from each of the second sense amplifiers;

a plurality of third holding circuits individually holding data output from the first holding circuits after being delayed by time that the read address gains with respect to the burst address;

a plurality of fourth holding circuits individually holding data output from the second holding circuits after one clock later than the third holding circuit;

a first decoder supplying data held in the third holding circuits to the first bus line;

a second decoder supplying data held in the fourth holding circuits to the second bus line; and

an output circuit connected to the first and second bus lines, and alternately outputting data transmitted from the first and second bus lines.

13. The device according to claim 12, wherein the first and second decoders operate at a two-clock cycle, and mutually have one-clock phase difference.

14. The device according to claim 12, wherein when the output circuit outputs desired data, the first and second decoders output the data to the first and second bus lines before one clock of the data output.

15. The device according to claim 12, wherein the first and second holding circuits comprise an asynchronous latch circuit, and the third and fourth holding circuits comprise a synchronous latch circuit.

16. A semiconductor memory device comprising:

first and second banks individually having a plurality of arrayed memory cells;

a first bus line transmitting even data read from the first bank, and having a bit width equivalent to one word;

a second bus line transmitting odd data read from the first bank and the redundancy memory, and having a bit width equivalent to one word;

a third bus line transmitting even data read from the second bank, and having a bit width equivalent to one word;

a fourth bus line transmitting odd data read from the second bank and the redundancy memory, and having a bit width equivalent to one word;

a first output circuit outputting even data read from a memory cell of the first bank in accordance with read address to the first bus line, and outputting odd data read from the memory cell of the first bank in accordance with read address to the second bus line;

a second output circuit outputting even data read from a memory cell of the second bank in accordance with read address to the third bus line, and outputting

odd data read from the memory cell of the second bank in accordance with read address to the fourth bus line; and

a third output circuit connected to the first to fourth bus lines, and alternately outputting the even and odd data from one of first and second bus lines and third and fourth bus lines corresponding to selected one of the first and second banks.

17. The device according to claim 16, wherein the first output circuit comprises:

a plurality of first sense amplifiers detecting even data read from a memory cell of the first bank in accordance with read address;

a plurality of second sense amplifiers detecting odd data read from the memory cell of the first bank in accordance with read address;

a plurality of first holding circuits individually holding data output from each of the first sense amplifiers;

a plurality of second holding circuits individually holding data output from each of the second sense amplifiers;

a plurality of third holding circuits individually holding data output from the first holding circuits after being delayed by time that the read address gains with respect to the burst address;

a plurality of fourth holding circuits

individually holding data output from the second holding circuits after one clock later than the third holding circuit;

a first decoder supplying data held in the third holding circuits to the first bus line; and

a second decoder supplying data held in the fourth holding circuits to the second bus line.

18. The device according to claim 17, wherein the second output circuit comprises:

a plurality of third sense amplifiers detecting even data read from a memory cell of the second bank in accordance with read address;

a plurality of fourth sense amplifiers detecting odd data read from the memory cell of the second bank in accordance with read address;

a plurality of fifth holding circuits individually holding data output from each of the third sense amplifiers;

a plurality of sixth holding circuits individually holding data output from each of the fourth sense amplifiers;

a plurality of seventh holding circuits individually holding data output from the fifth holding circuits after being delayed by time that the read address gains with respect to the burst address;

a plurality of eighth holding circuits individually holding data output from the sixth holding

circuits after one clock later than the third holding circuit;

a third decoder supplying data held in the seventh holding circuits to the third bus line; and

a fourth decoder supplying data held in the eighth holding circuits to the fourth bus line.

19. The device according to claim 17, wherein the first and second decoders operate at a two-clock cycle, and mutually have one-clock phase difference.

20. The device according to claim 18, wherein the third and fourth decoders operate at a two-clock cycle, and mutually have one-clock phase difference.